

SBND FEMB Teststand

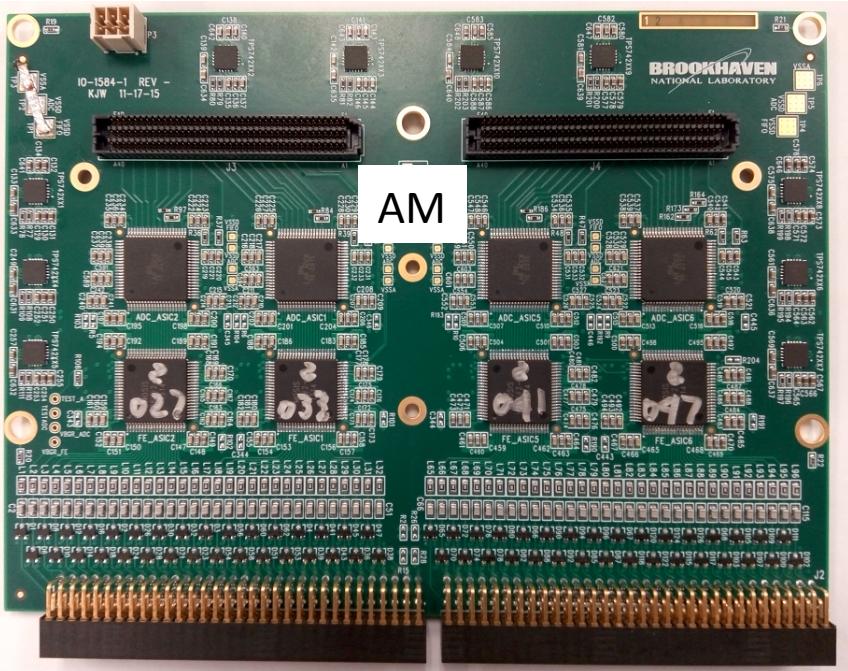
User Guide

Shanshan Gao

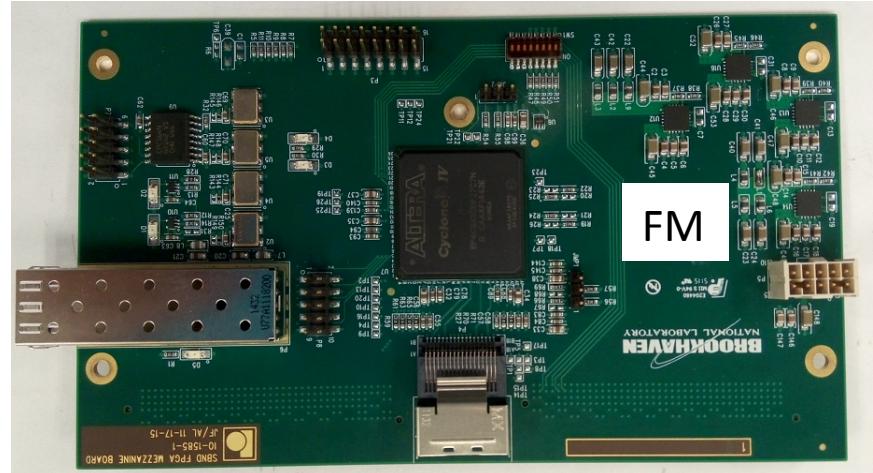
6/18/16

FEMB: Front End Mother Board

- SBND FEMB
 - AM: Analog Mother Board
 - 8 FE ASICs & 8 V* ADC ASICs
 - 128 FE channels
 - Cold regulators: TI TPS74201
 - FM: FPGA mezzanine
 - Cyclone IV GX FPGA
 - MiniSAS connector
 - Toy TPC
 - Emulate detector capacitance

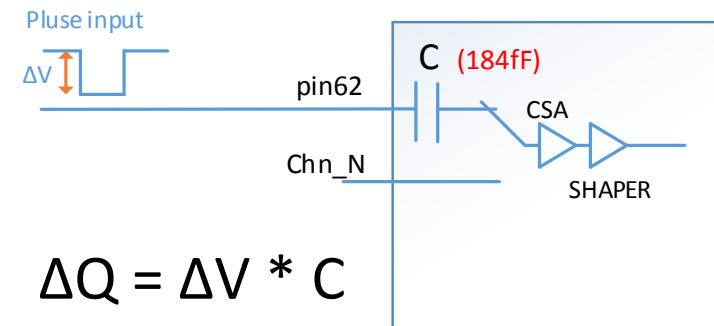
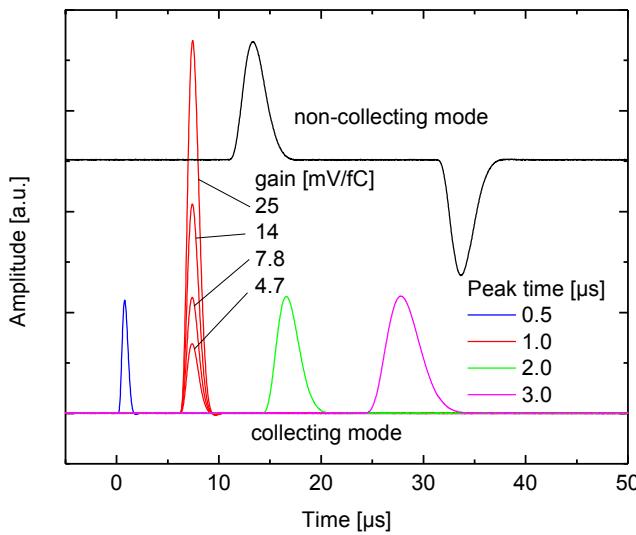


Toy TPC: 150pF

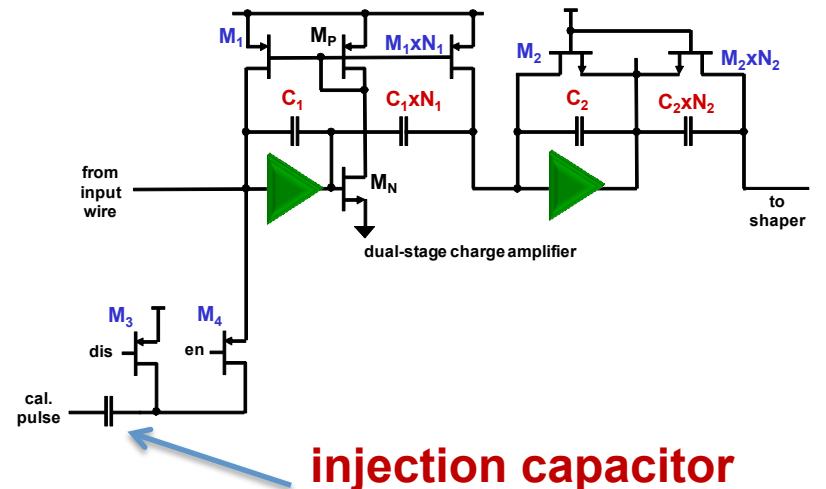


FE-ASIC calibration and ENC calculation

- Calibration
 - Step voltages generated by FPGA "DAC"
 - Capacitor is integrated in FE ASIC
 - Next version FE ASIC will include integrated calibration injection circuit
- ENC calculation
 - 250,000 samples per channel to calculate rms noise

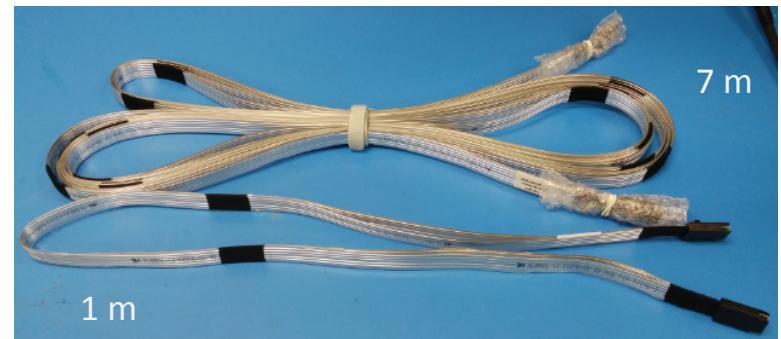
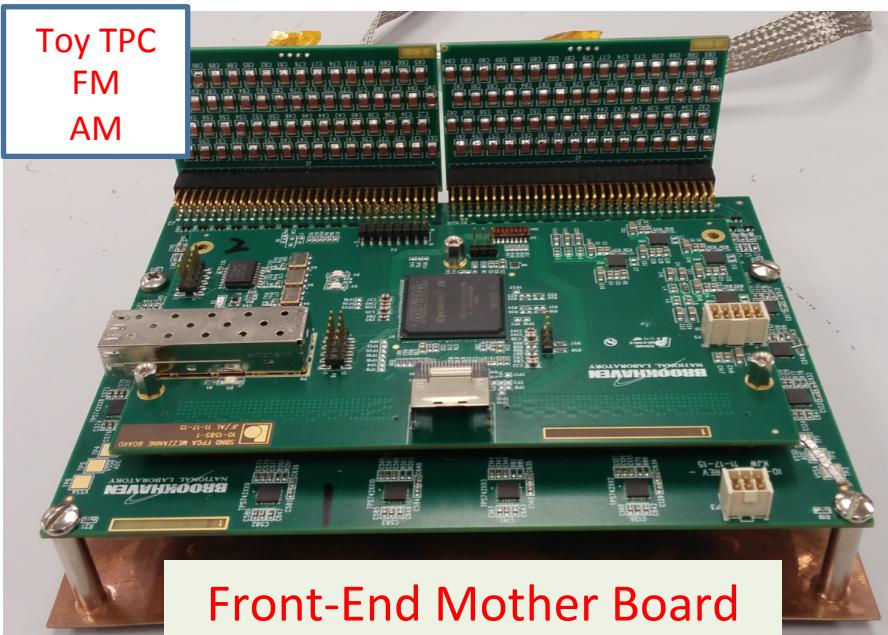


$$\Delta Q = \Delta V * C$$



injection capacitor
measured: **184 fF at 300 K**
183 fF at 77 K (0.5 %)

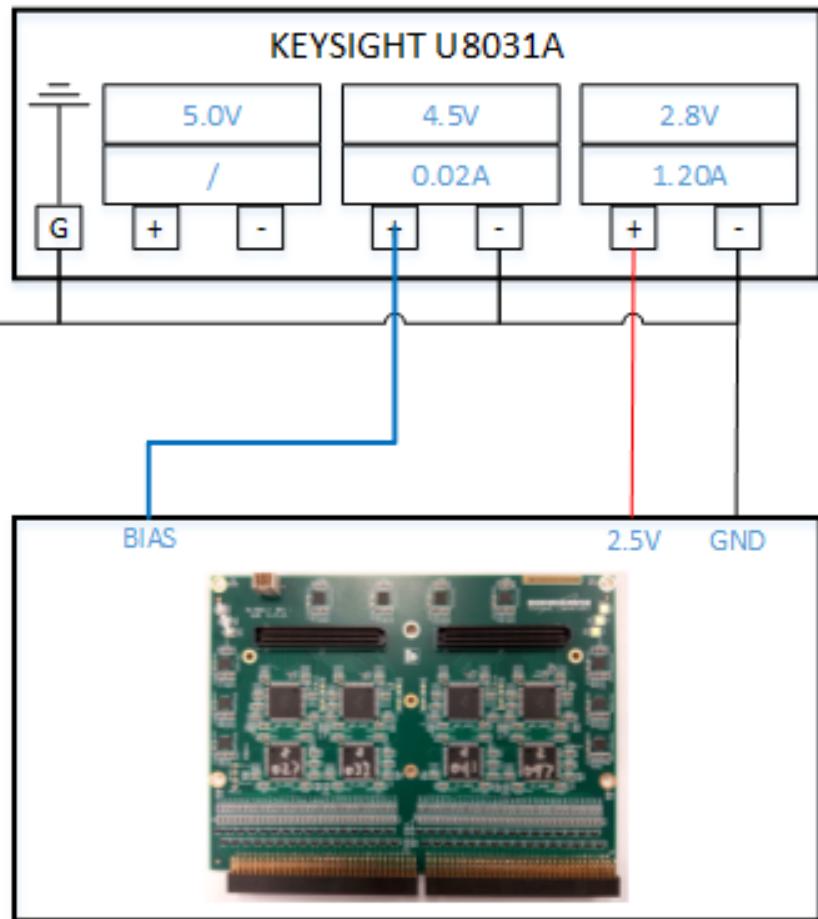
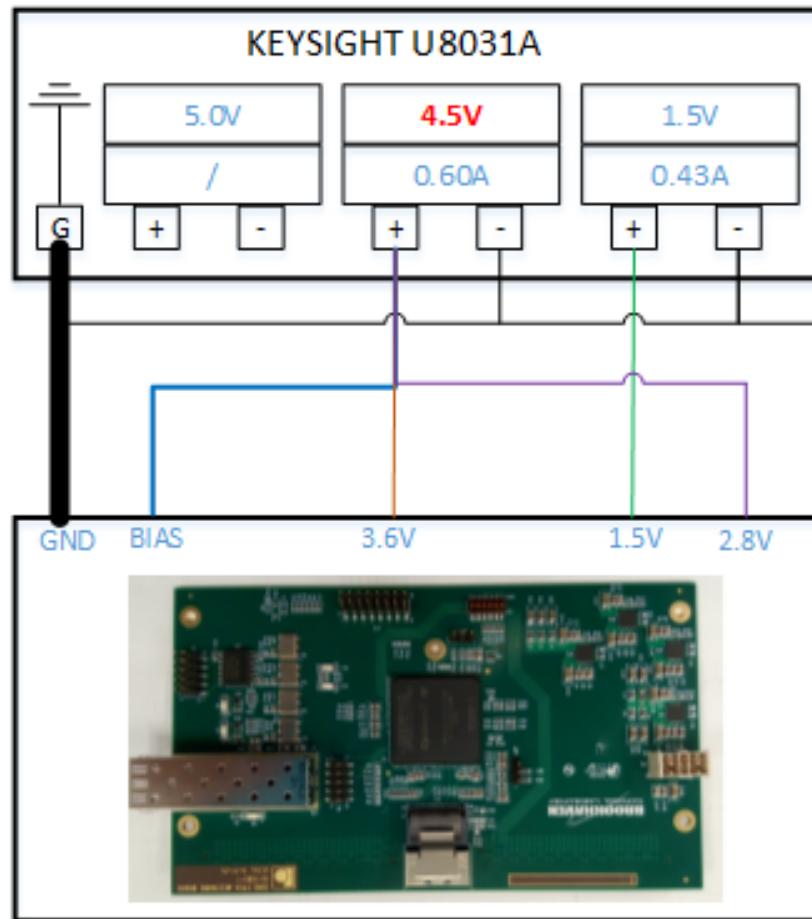
Front End Electronics



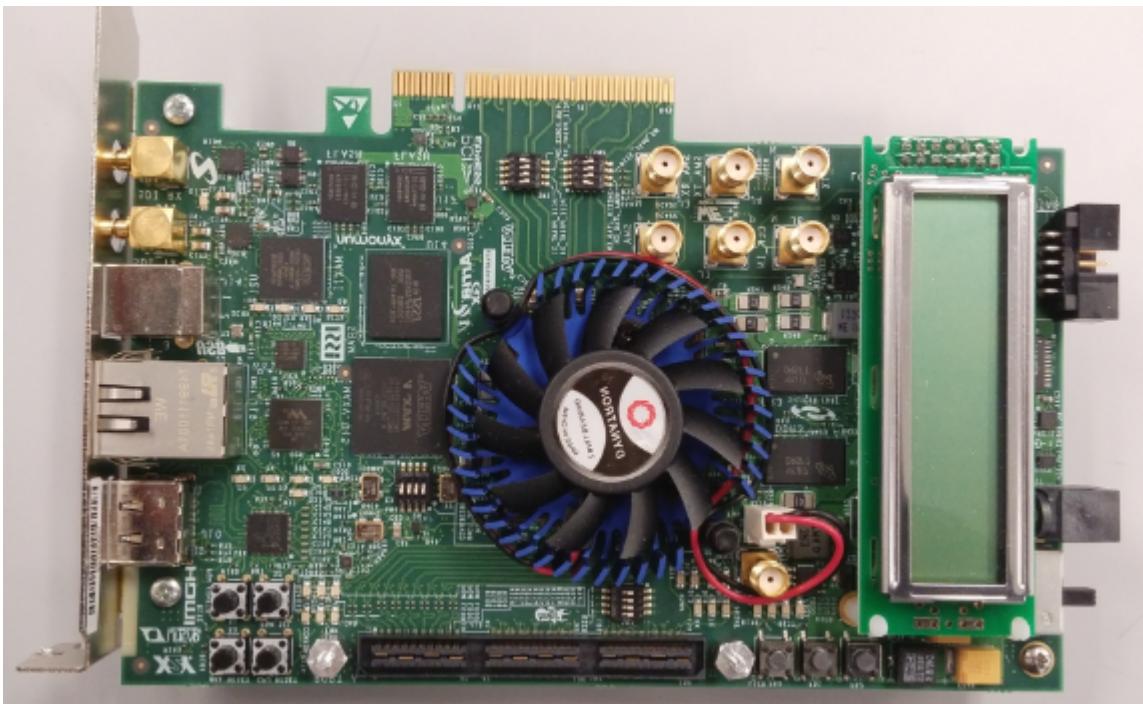
3M miniSAS cable

Front End electronics will be tested at room and LN2 temperature.

Power Supply Scheme



Warm Readout Electronics



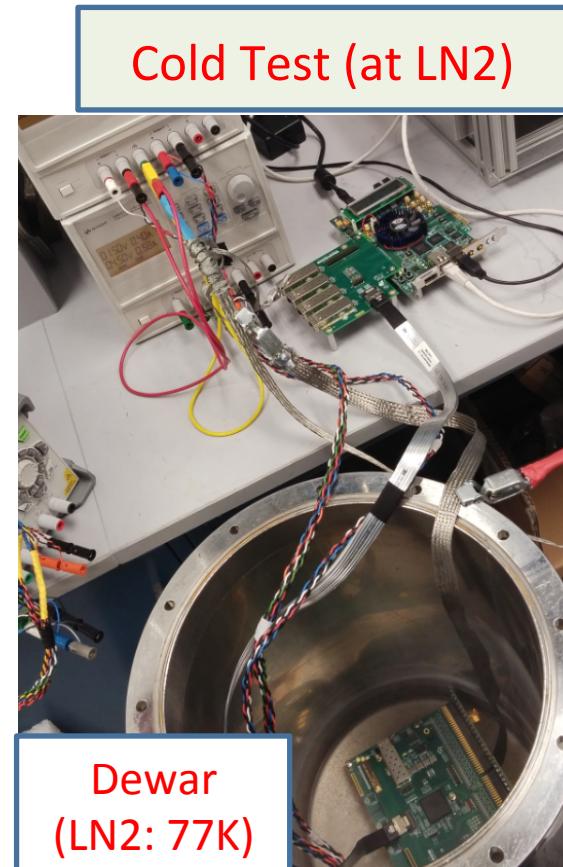
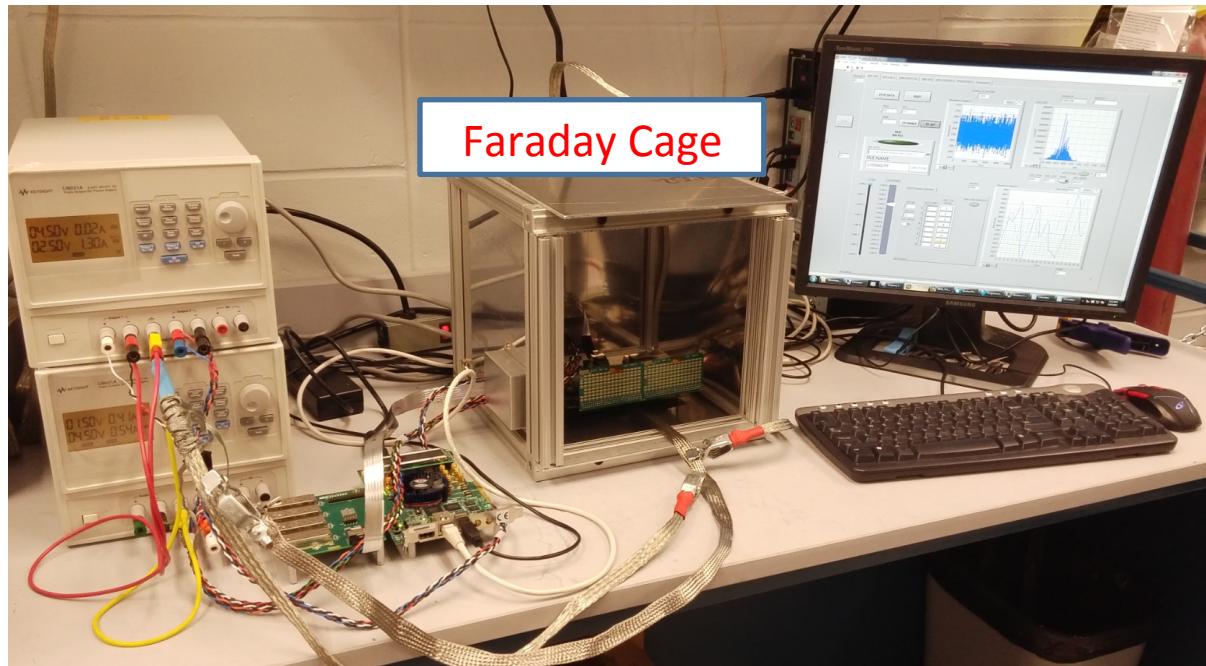
Altera Arria V Board



SBND Test Board

Warning: never turn off Arria V Board.

Test Setup

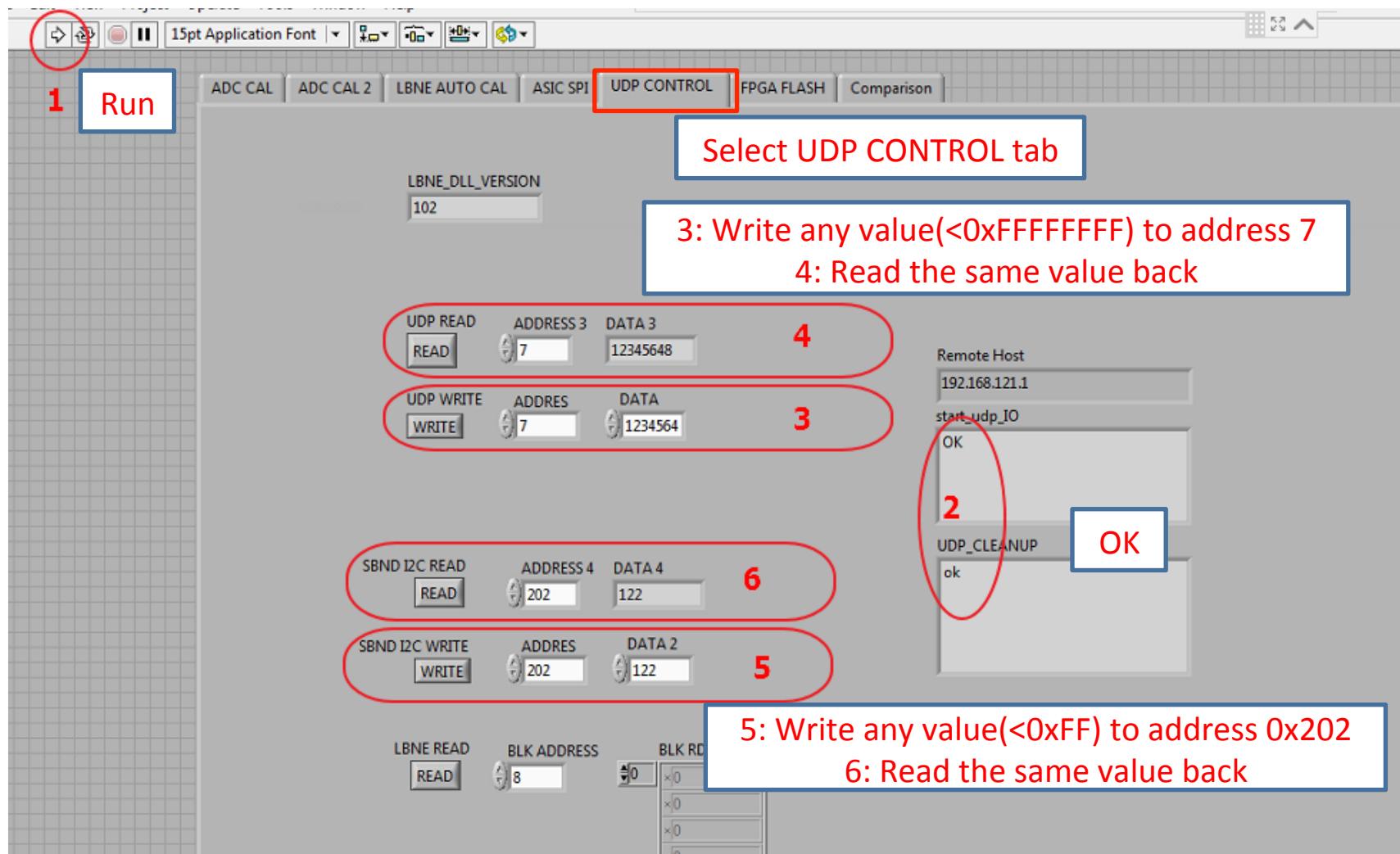


Warm Test (at RT)

Preparation

1. Is Arria V board power on?
No: Get Shanshan for help.
2. Check Ethernet cable connection from Arria V board to computer
3. Check LV power cable connection to FEMB
4. Check miniSAS data cable from Arria V board to FEMB
5. Turn on LV power: both U8031A → “All on”
Check the current value:
 1. Upper supply: 4.5V: <0.03A; 2.8V: <1.10A (when first powered on)
 2. Lower supply: 4.5V: <0.65A; 1.5V: <0.5A
6. Start LabView GUI: double click “SBND_TST.vi”
Path: D:\FEMB_TEST_Setup\SBND_TST.vi
7. Check UDP communication (next slide)
8. Check the I2C communication between Arria V board and FEMB (next slide)

UDP/I2C Communication in LabView



Troubleshooting

- If the Labview GUI crashes at any point:
 - Restart it and repeat the UDP/I2C communication test
- If start_udp_IO is not OK in step 2:
 - Double check the Ethernet cable is connected
- If UDP readback fails in step 4:
 - Double check the Ethernet cable is connected
- If UDP readback succeeds in step 4, but I2C readback fails in step 6:
 - Double check the miniSAS data cable is connected

Data Acquisition Process

1. Configure FE ASICs and ADCs

Slide 12

2. Phase adjustment

Slide 14

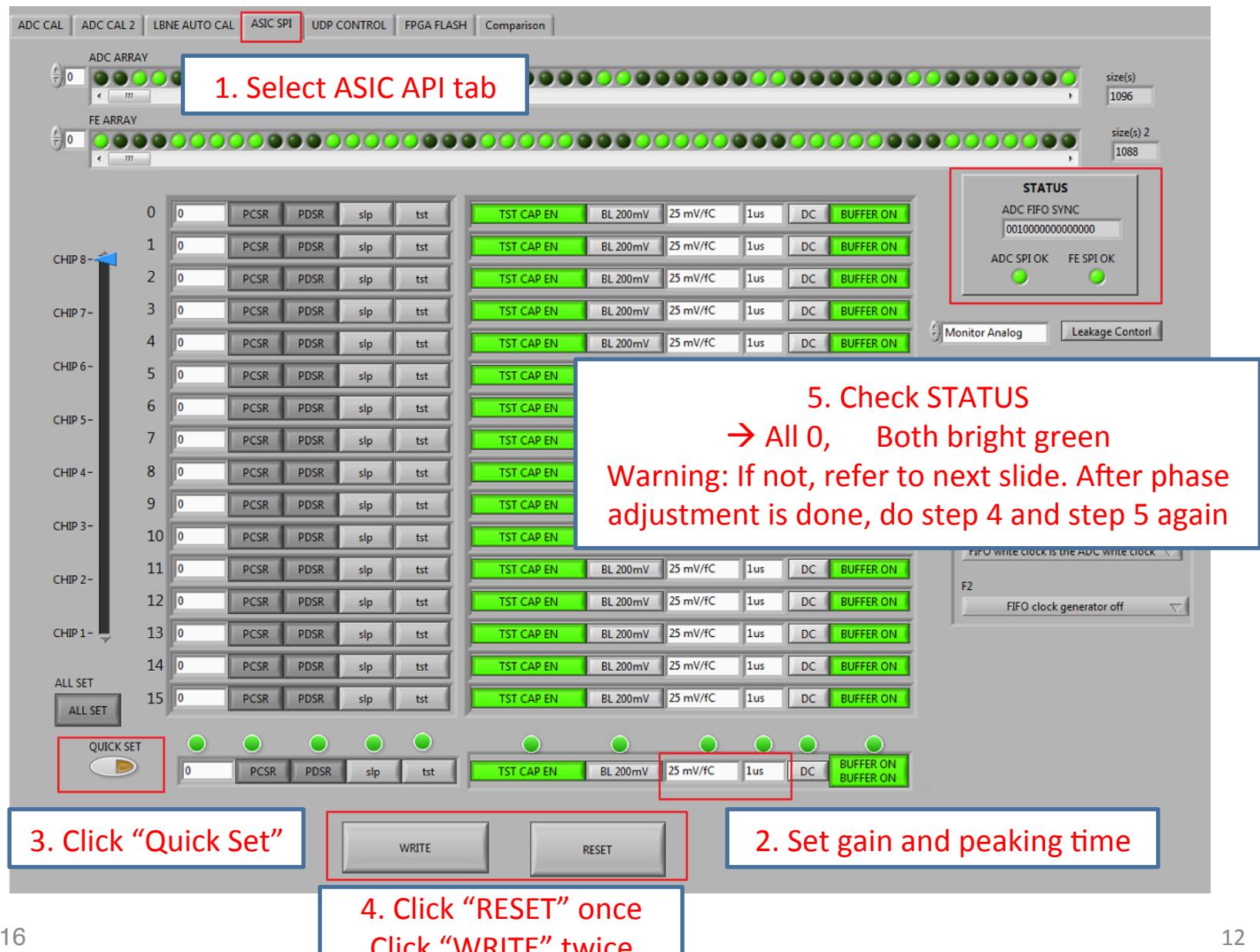
3. Live view

Slide 15

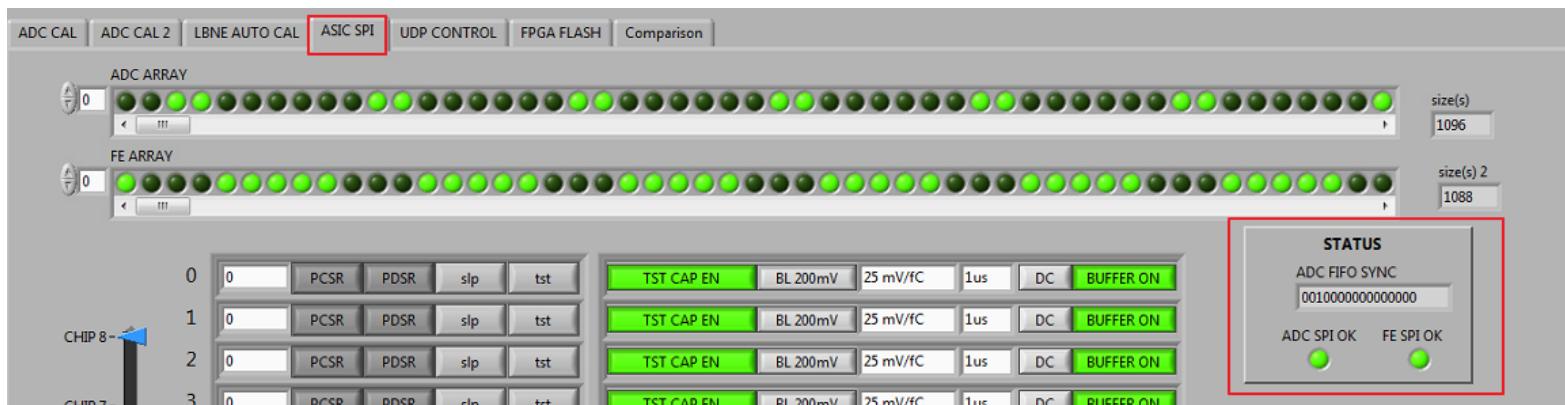
4. Automatic data-taking

Slide 16

FE and ADC ASIC Configuration



ASIC Configuration Troubleshooting



1. SPI check

If ADC SPI OK or FE SPI OK are not green, downloading the SPI chain to one or more ASIC has failed. Repeat the RESET and 2xWRITE clicks below. If either remains grey after several tries, get Shanshan for help.

2. ADC FIFO SYNC check

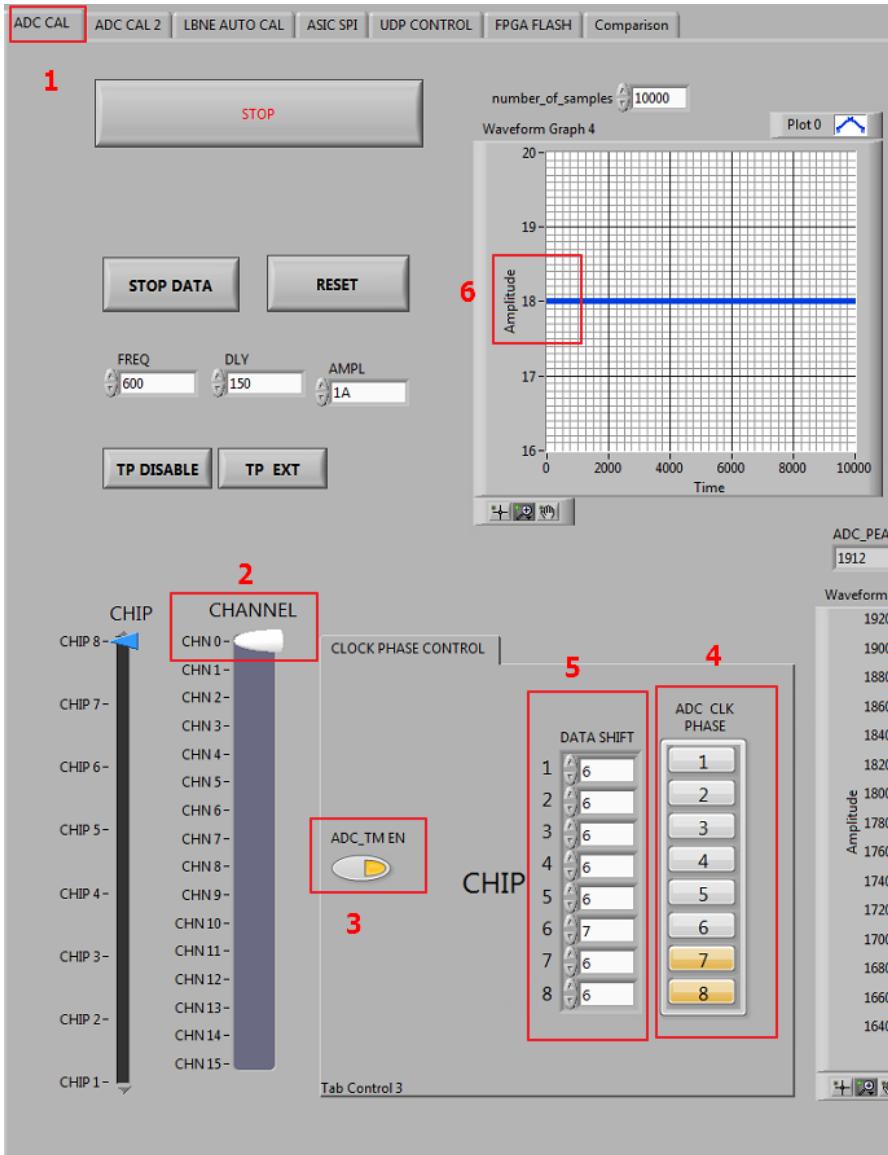
The ADC FIFO SYNC is controlled by a phase adjustment. Each ADC FIFO has two halves, one for the lower 8 channels and one for the upper 8 channels. If any bit in the ADC FIFO SYNC is 1, then one half of an ADC FIFO is out of phase. The ADC FIFO bit order is:

0000000000000000
 \u25b6 \u25b6
 ADC 8 upper/lower ... 7 2 ... ADC 1 upper/lower

To get the ADC FIFOs in phase, read off which ADCs are out of SYNC in the bit pattern and do the phase adjustment on the next slide for those ADCs.

Click "RESET" once
Click "WRITE" twice

Phase Adjustment



If the STATUS box for the ASIC configuration is OK, don't change anything.

1. Select ADC CAL tab
 2. Select CHIP and CHANNEL
Use CHN0 to check the lower channels or CHN8 to check the upper channels in the ADC FIFO
 3. Click "ADC_TM EN"
 4. Toggle ADC CLK PHASE for the ASIC that is out of sync and check step 6
If step 4 doesn't work, adjust the DATA SHIFT and check step 6
 5. If step 4 doesn't work, adjust the DATA SHIFT and check step 6
 6. Each half of the ADC FIFO sends a **known** value when it is in SYNC:
CHN0 must be 18 for the lower
CHN8 must be 2200 for the upper
- Once the values in CHN0 and CHN8 are correct for all ASICs, unselect ADC_TM EN and repeat the FE and ADC configuration in slide 12.

Live View

- Real-time waveform

- Select the ADC CAL tab
 - Toggle to “TP DISABLE”, “FPGA DAC”
 - Select a chip and channel

- FFT

- Select the ADC CAL 2 tab
 - Real-time FFT of chip and channel selected in ADC CAL

- Test pulse

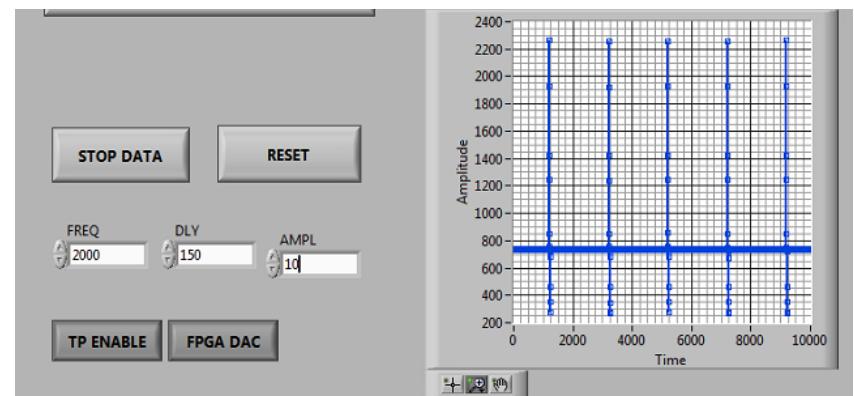
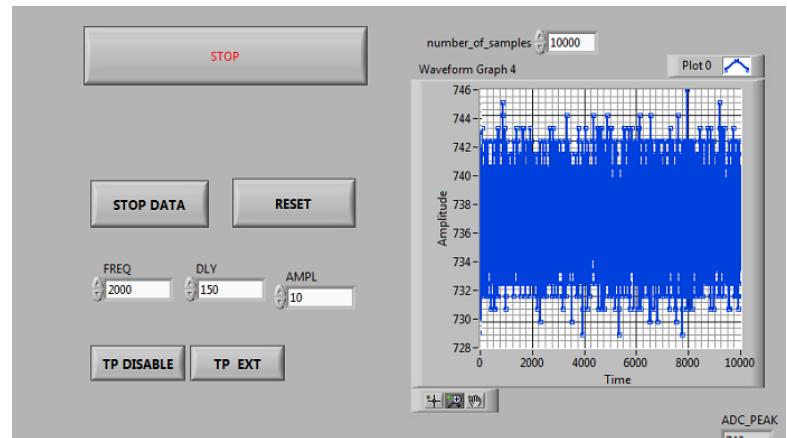
- Toggle to “TP ENABLE”, “FPGA DAC”
 - Frequency: set FREQ to any value from 100 to 10000
 - Amplitude: set AMPL

Suggested settings:

- Gain = 4.7 mV/fC, AMPL = 0x10
 - Gain = 7.8 mV/fC, AMPL = 0x0B
 - Gain = 14 mV/fC, AMPL = 0x08
 - Gain = 25 mV/fC, AMPL = 0x04

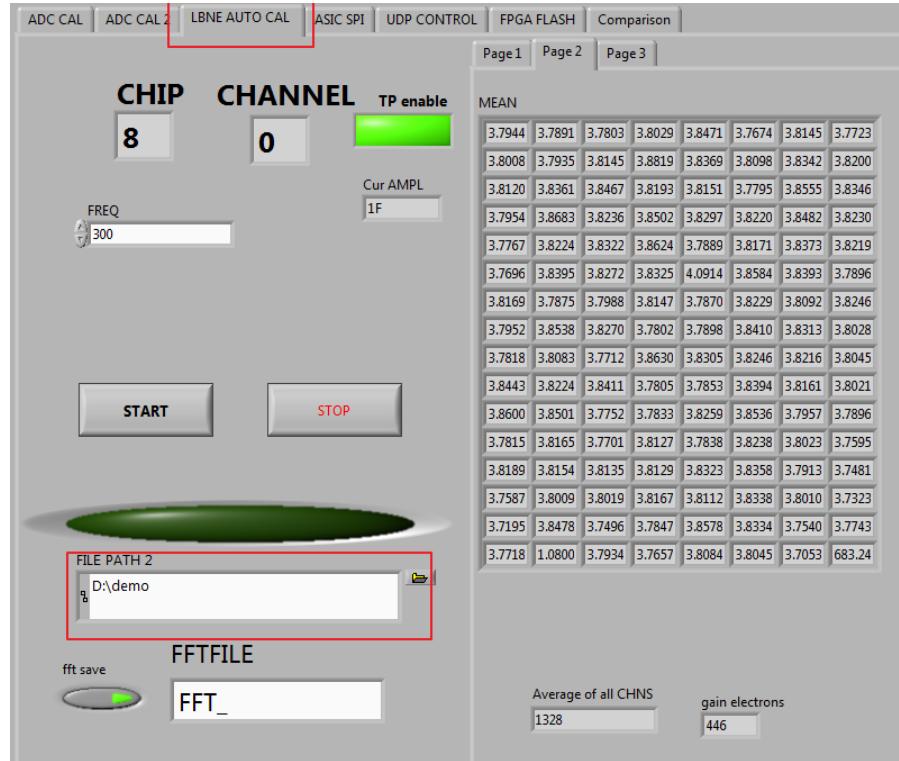
- Delay: set DLY from 1 to 0xff

- To lock the peak of shaper, adjust DLY until the Gaussian waveform is symmetric



Automatic Data-Taking

- Select the LBNE AUTO CAL tab
- Choose a file path
 - Click on the folder icon
 - Select “D:\demo”



- Take data
 - Click START
 - If the shaper peak is locked, click YES
 - See DLY setting in slide 15
 - Data should start appearing in D:\demo\ggs in 2 Excel spreadsheets
 - gg = gain value of 47, 78, 14, or 25 and s = shaping value of 0, 1, 2, 3
 - Data-taking should take about 5 minutes to finish
 - Click STOP at any time to end data-taking

Example Data Analysis

1. Copy data to analysis demo folder
 1. Path: D:\FEMB_TEST_Setup\python_demo\input
 2. test_mean_mmdd_ttttt.xlsx
 3. test_rms_mmdd_ttttt.xlsx

m = month, d = day, and t = time
2. Edit analysis script: “Main.py”
 1. Path: D:\FEMB_TEST_Setup\python_demo\Main.py
Double click on Main.py to open it in VI
 2. Change **date_time** variable to match **mmdd_ttttt**
3. Run the analysis script
 1. Click “ALT + F5” in Main.py
Close the pop-up window and VI editor when complete
4. View the result
 1. Path: D:\FEMB_TEST_Setup\python_demo\output
 2. Check gain.jpg and rms.jpg
Some of the channels on this FEMB are dead; which ones?

Exercises

- Compare RMS noise between different peaking times
- Compare gain between different gain settings

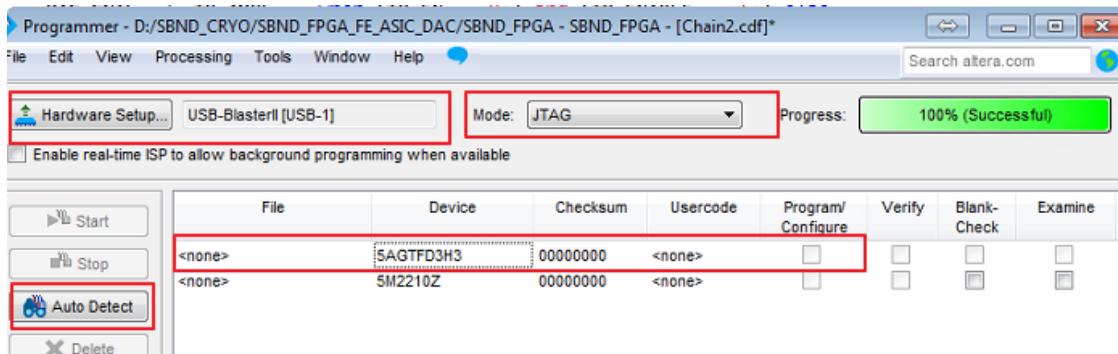
Backup

- How to download firmware for Arria V board

1. Open Quartus Prime 15.1 Programmer on PC
2. Download firmware
 1. Select USB-Blaster II
 2. JTAG
 3. Auto Detect
 4. Right click → change file

Select : D:\FEMB_TEST_Setup\Arria_V_firmware\A5GX_SBND_TRAN.sof

5. Enable Program/Configure for device 5AGXFB3H4F35



File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine	Security Bit	Erase	ISP CLAMP	IPS File
..../FEMB_TEST_Setup/A...	5AGXFB3H4F35	0440C48C	0440C48C	<input checked="" type="checkbox"/>	<input type="checkbox"/>						
<none>	5M2210Z	00000000	<none>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	

